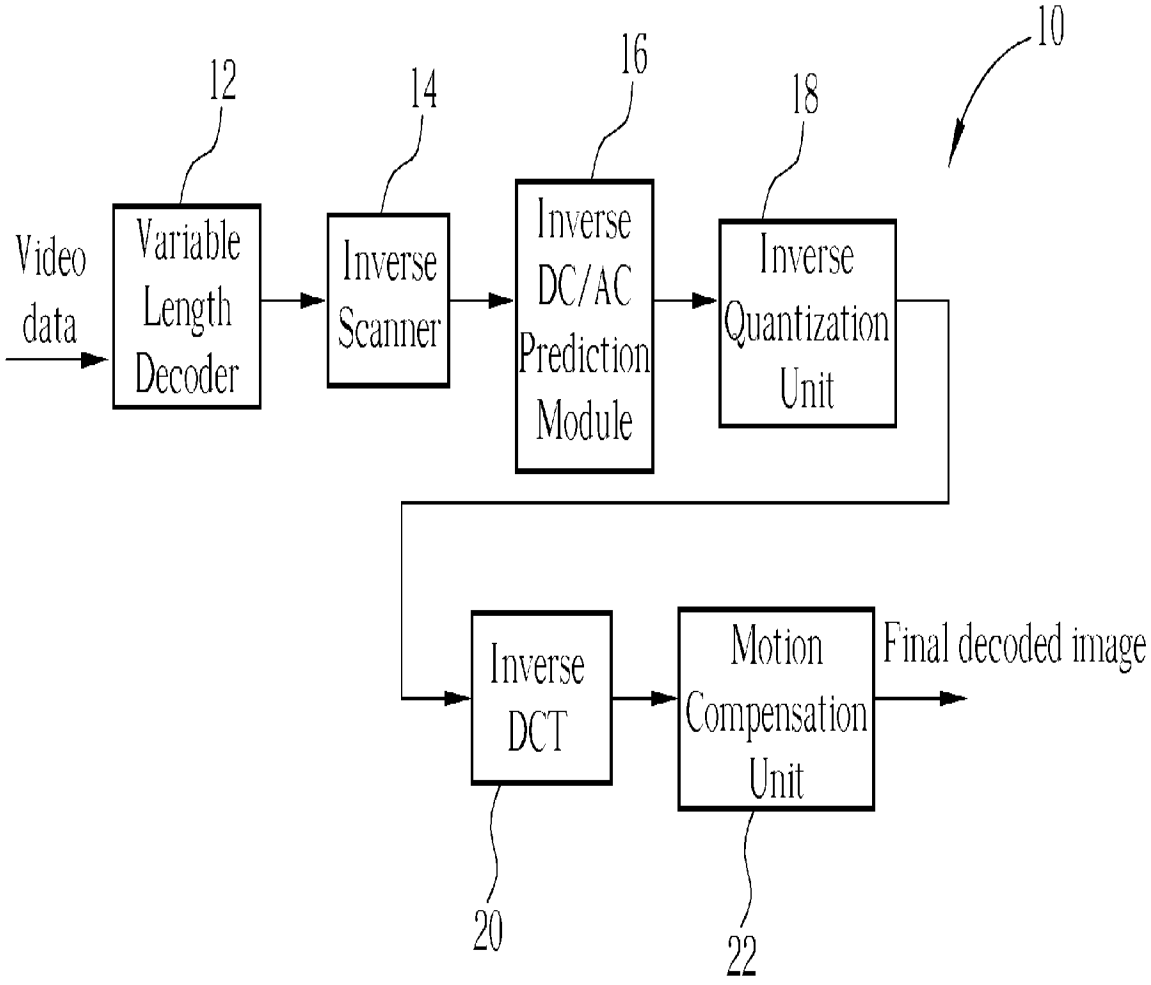

Fig. 1 Related Art

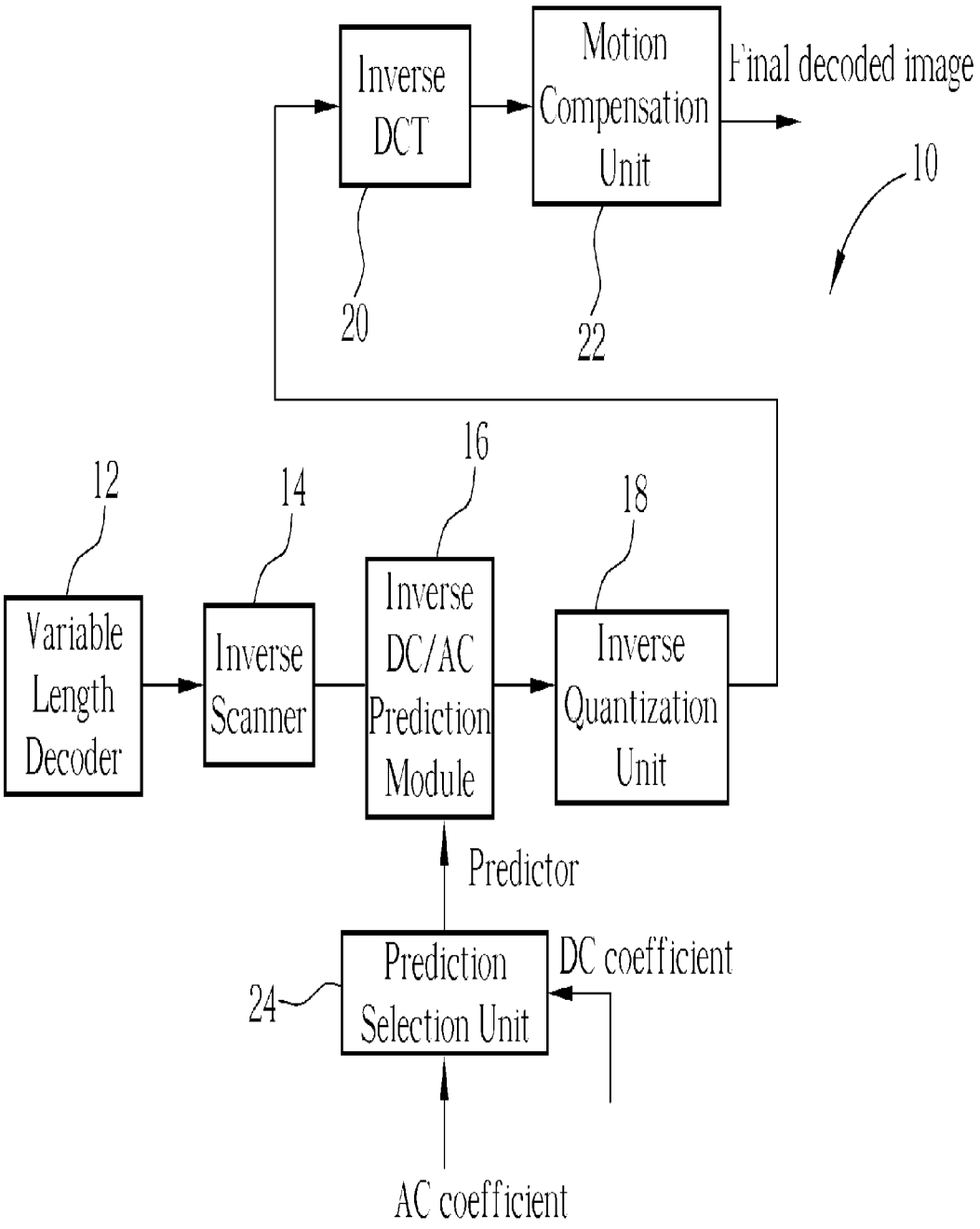

Fig. 2 Related Art

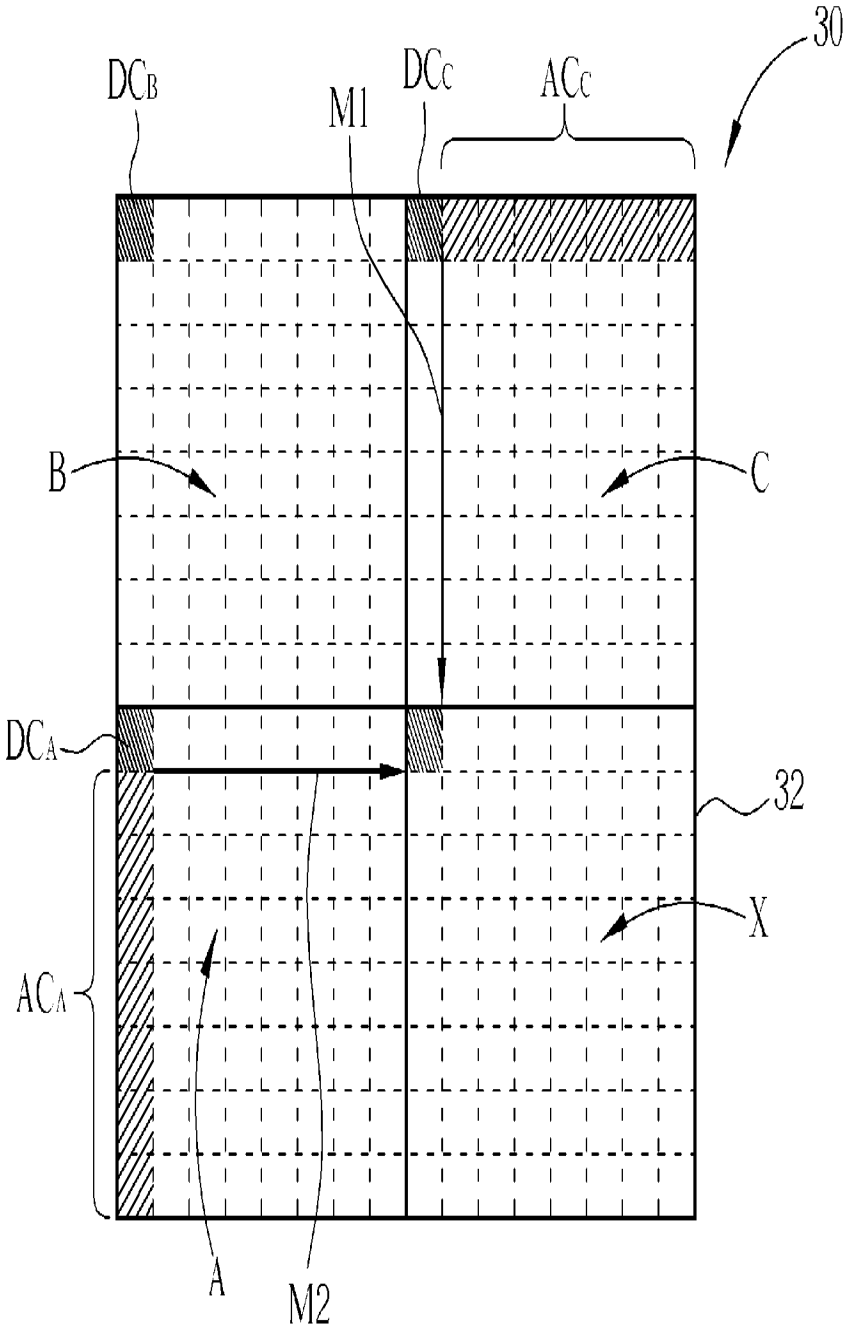

Fig. 3 Related Art

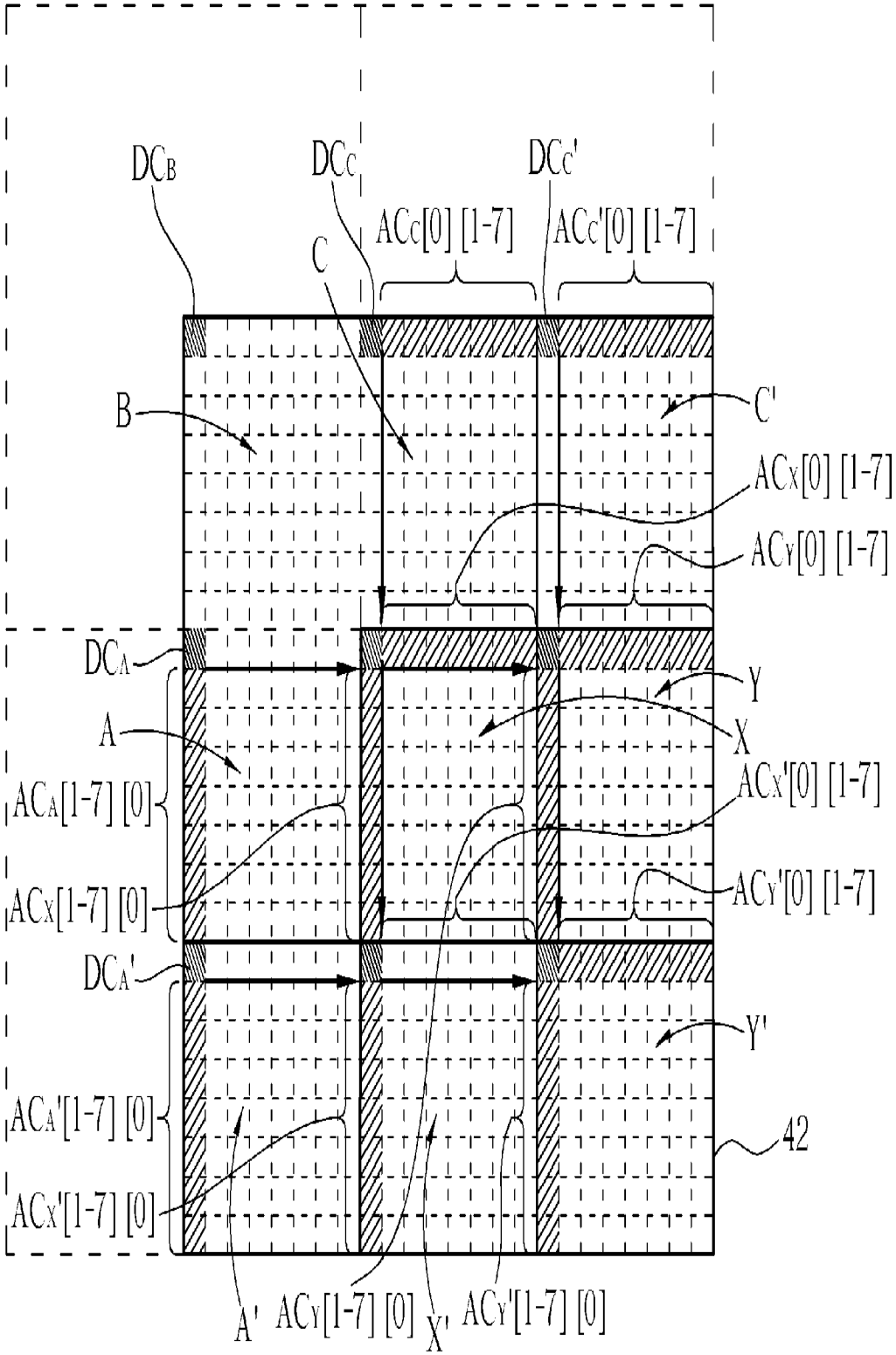

Fig. 4 Related Art

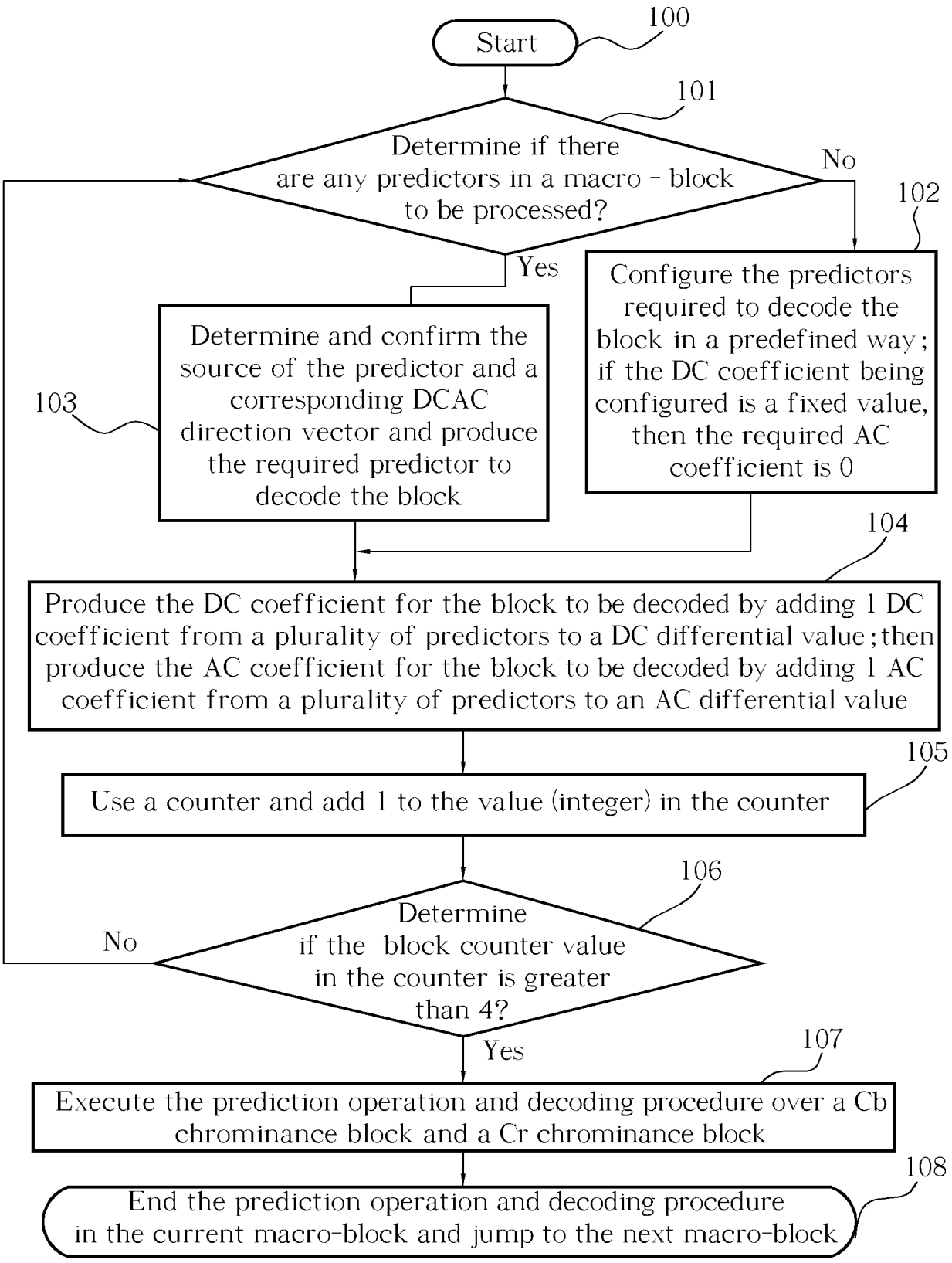

Fig. 5 Related Art

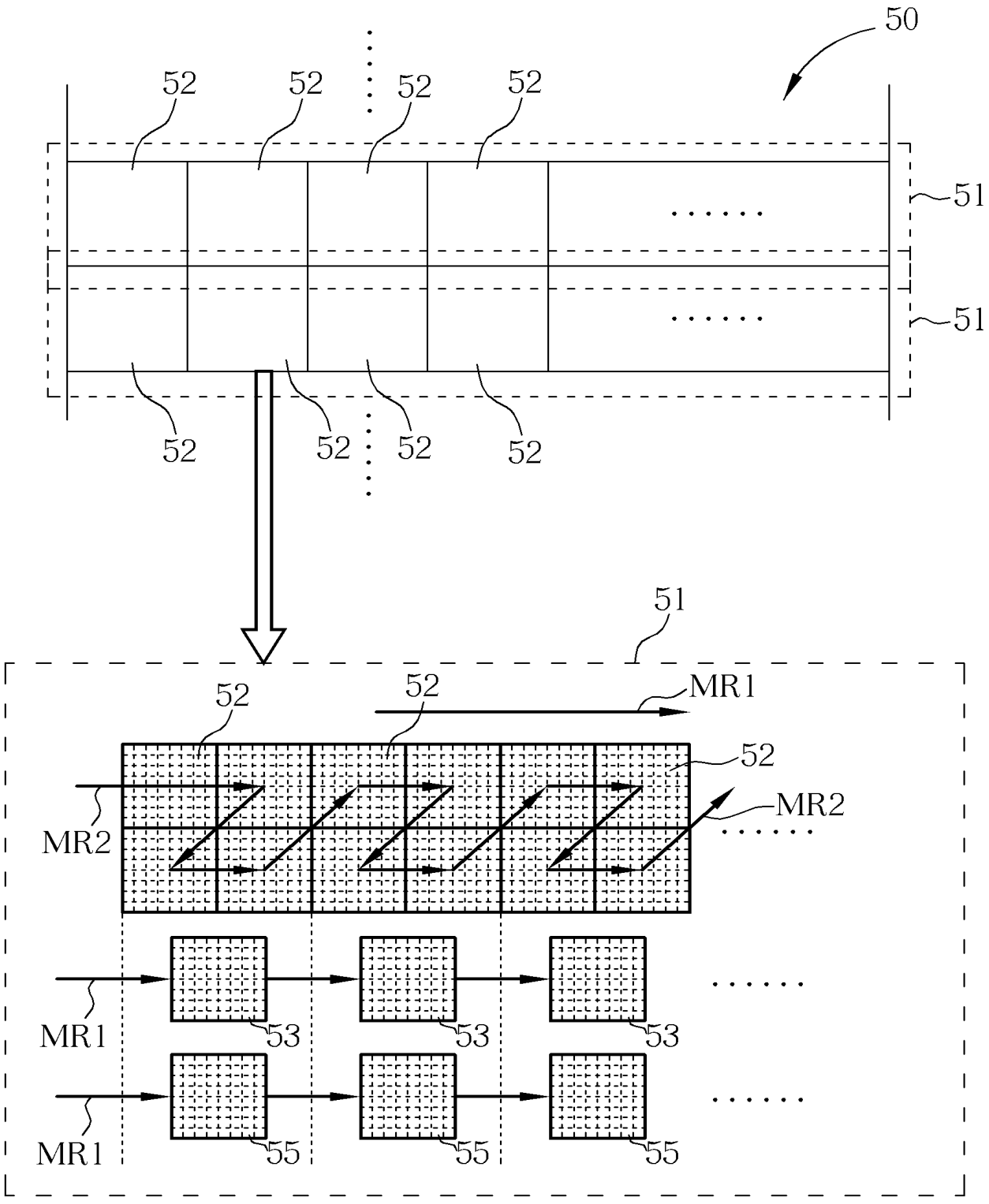
50
52
52
52
52
51
51
52
52
52
52
51
52
52
MR1
52
MR2
MR2
MR1
53
53
53
MR1
55
55
55

Fig. 6

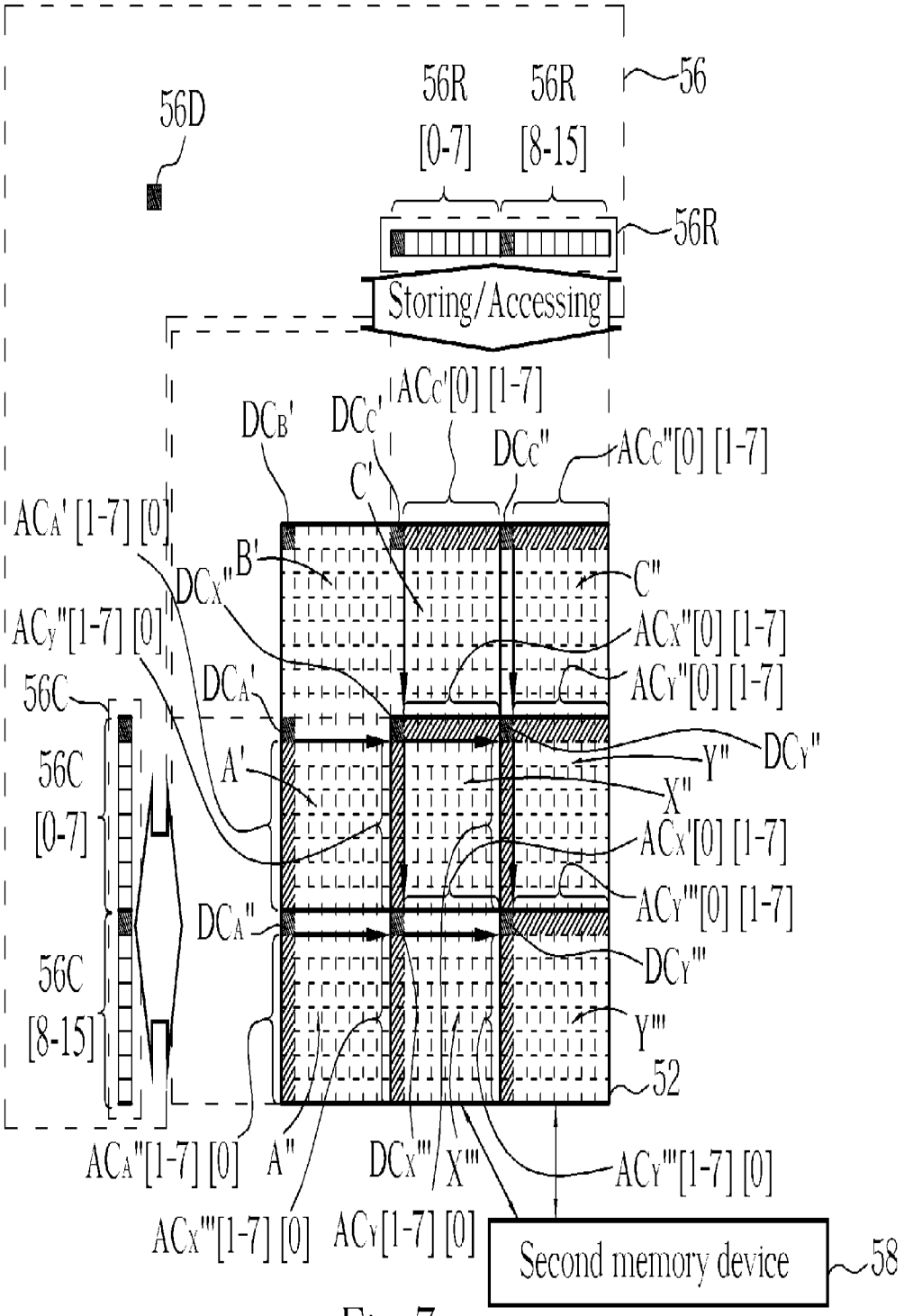
56
56R
[0-7]
56R
[8-15]
56D
56R
Storing/Accessing
ACC'[0] [1-7]
DCB'
DCC'
DCC"
ACC"[0] [1-7]
C'
ACA' [1-7] [0]
B'
DCX"
C"
ACY"[1-7] [0]
ACX"[0] [1-7]
ACY"[0] [1-7]
56C
DCA'
56C
[0-7]
A'
Y"
DCY"
X"
ACX'[0] [1-7]
ACY'"[0] [1-7]
DCA"
DCY'"
56C
[8-15]
Y'"
52
ACA"[1-7] [0]
A"
DCX'"
X'"
ACY'"[1-7] [0]
ACX'"[1-7] [0]
ACY[1-7] [0]
Second memory device
58

Fig. 7

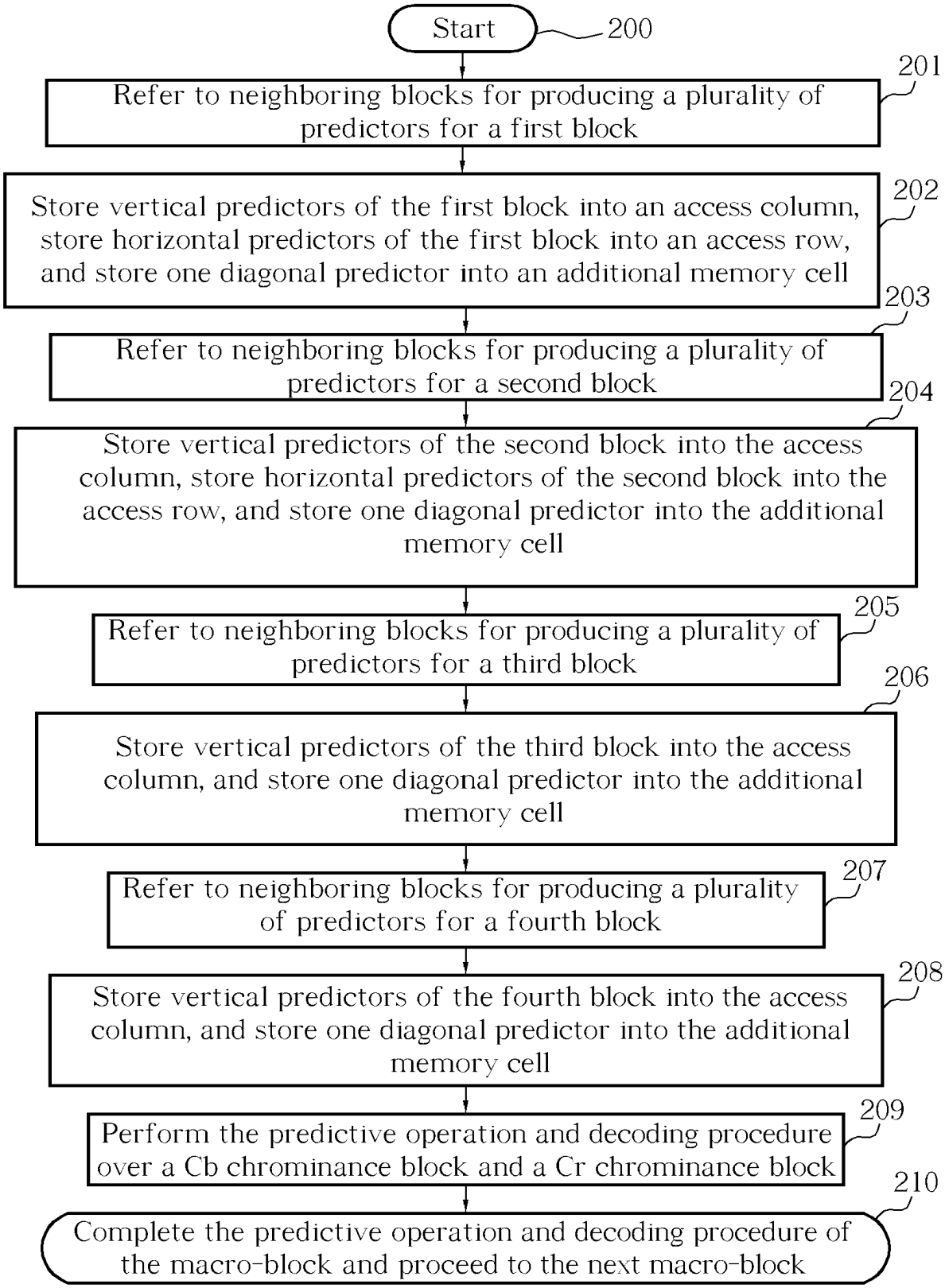
Start
200
Refer to neighboring blocks for producing a plurality of predictors for a first block
201
Store vertical predictors of the first block into an access column, store horizontal predictors of the first block into an access row, and store one diagonal predictor into an additional memory cell
202
Refer to neighboring blocks for producing a plurality of predictors for a second block
203
Store vertical predictors of the second block into the access column, store horizontal predictors of the second block into the access row, and store one diagonal predictor into the additional memory cell
204
Refer to neighboring blocks for producing a plurality of predictors for a third block
205
Store vertical predictors of the third block into the access column, and store one diagonal predictor into the additional memory cell
206
Refer to neighboring blocks for producing a plurality of predictors for a fourth block
207
Store vertical predictors of the fourth block into the access column, and store one diagonal predictor into the additional memory cell
208
Perform the predictive operation and decoding procedure over a Cb chrominance block and a Cr chrominance block
209
Complete the predictive operation and decoding procedure of the macro-block and proceed to the next macro-block
210

Fig. 8

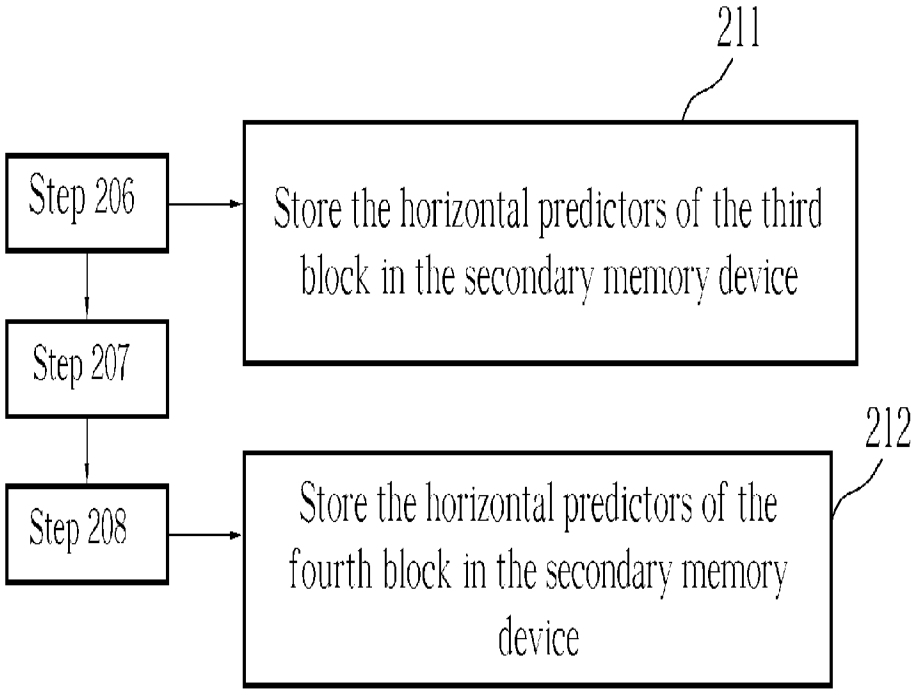
211
Step 206
Store the horizontal predictors of the third block in the secondary memory device
Step 207
212
Step 208
Store the horizontal predictors of the fourth block in the secondary memory device

Fig. 9

Content for storing / Sequence of decoding (from up to down)	Access column 56C[0-7]	Access column 56C[8-15]	Access row 56R[0-7]	Access row 56R[8-15]	Memory cell 56D
First block X"	DC_A' and $AC_A'[1-7][0]$	DC_A'' and $AC_A''[1-7][0]$	DC_C' and $AC_C'[0][1-7]$	DC_C'' and $AC_C''[0][1-7]$	DC_B'
Second block Y"	(Updated) DC_X'' and $AC_X''[1-7][0]$	DC_A'' and $AC_A''[1-7][0]$	(Updated) DC_X'' and $AC_X''[0][1-7]$	DC_C'' and $AC_C''[0][1-7]$	DC_C'
Third block X"'	(Updated) DC_Y'' and $AC_Y''[1-7][0]$	DC_A'' and $AC_A''[1-7][0]$	DC_X'' and $AC_X''[0][1-7]$	(Updated) DC_Y'' and $AC_Y''[0][1-7]$	DC_A'
Fourth block Y"'	DC_Y'' and $AC_Y''[1-7][0]$	(Updated) DC_X''' and $AC_X'''[1-7][0]$	DC_X'' and $AC_X''[0][1-7]$	DC_Y'' and $AC_Y''[0][1-7]$	DC_X''

Fig. 10